

EAST - [09945500.wsp.1] [x]

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Drafts
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 L1: (19) US-6101131-S.DID. OR US-6127227-S.DID. OR US-616
 L5: (0) L1 and (flash nonvolatile (non adj volatile)) and
 L6: (3) L1 and (flash nonvolatile (non adj volatile)); and
 Failed
 Saved
 (9) ((pillar with substrate) and (control\$4 adj2 gate) and
 (96) (pillar with substrate) and (control\$4 near3 gate) and
 (2645) pillar with substrate
 (85) (pillar with substrate) and (control\$4 adj2 gate) and
 (28) ((pillar with substrate) and (control\$4 near3 gate)
 (9) ((pillar with substrate) and (control\$4 near3 gate) and
 (15) (pillar with substrate) and (program\$5 near2 decod\$3
 (41) (pillar with substrate) and (program\$5 with decod\$3
 (24) low adj2 tunnel adj2 barrier
 (537) programmable adj2 decoder
 (424) (programmable adj2 decoder) and memory
 (17) ((programmable adj2 decoder) and memory) and (vertical
 (4) 6210999.pn. 6541280.pn.

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Search Operator: OR Exact Match High Quality Results

L1 and (flash nonvolatile (non adj volatile)) and (vertical adj2 (channel gate pillar))

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#	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	V	T	M
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6475857 B1	20021105	20	Method of making a scalable two transistor memory device	438/240	438/258		Kim, Woosik et al.	<input type="checkbox"/>					
2	<input type="checkbox"/>	<input type="checkbox"/>	US 5617351 A	19970401	19	Three-dimensional direct-write EEPROM arrays	365/185.05	257/298; 257/302;		Bertin, Claude L. et al.	<input type="checkbox"/>					
3	<input type="checkbox"/>	<input type="checkbox"/>	US 5455792 A	19951003	21	Flash EEPROM devices employing mid channel	365/185.15	257/316; 257/319;		Yi, Yong-Wan	<input type="checkbox"/>					

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Detailed View											
U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C
1	<input type="checkbox"/>	US 20030087495 A1	20030508	17	Memory address decode array with vertical transistors	438/295			Forbes, Leonard et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
2	<input type="checkbox"/>	US 20030047756 A1	20030313	35	Programmable memory address and decode circuits with	257/200			Forbes, Leonard	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
3	<input type="checkbox"/>	US 20030043632 A1	20030306	37	Programmable memory address and decode circuits with low	365/185.28			Forbes, Leonard	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
4	<input type="checkbox"/>	US 20030040157 A1	20030227	33	Vertical transistor with horizontal gate layers	438/268	257/E29.306; 438/270		Forbes, Leonard	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
5	<input type="checkbox"/>	US 20030038316 A1	20030227	34	Vertical transistor with horizontal gate layers	257/331	257/E29.306		Forbes, Leonard	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
6	<input type="checkbox"/>	US 2003006446 A1	20030109	37	Memory address and decode circuits with ultra thin	257/302			Forbes, Leonard et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
7	<input type="checkbox"/>	US 20020110039 A1	20020815	37	MEMORY ADDRESS AND DECODE CIRCUITS WITH ULTRA THIN	365/230.06	257/296; 365/230.01		Forbes, Leonard et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
8	<input type="checkbox"/>	US 20020109138 A1	20020815	35	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH	257/51			Forbes, Leonard	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
9	<input type="checkbox"/>	US 6597037 B1	20030722	32	Programmable memory address decode array with vertical	257/330	257/302; 257/319;		Forbes, Leonard et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
10	<input checked="" type="checkbox"/>	US 6566682 B2	20030520	33	Programmable memory address and decode circuits with	257/51	257/302; 365/230.02;		Forbes, Leonard	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
11	<input checked="" type="checkbox"/>	US 6498065 B1	20021224	22	Memory address decode array with vertical transistors	438/259	438/270		Forbes, Leonard et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
12	<input checked="" type="checkbox"/>	US 6446601 B1	20020910	35	Memory address and decode circuits with ultra thin	257/302	257/51		Forbes, Leonard et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
13	<input checked="" type="checkbox"/>	US 6153468 A	20001128	29	Method of forming a logic	438/257	257/E27.103; 438/165		Forbes, Leonard et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

L Number	Hits	Search Text	DB	Time stamp
1	537	programmable adj2 decoder	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/11 13:56
2	424	(programmable adj2 decoder) and memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/11 13:56
3	17	((programmable adj2 decoder) and memory) and (vertical adj3 (pillar gate channel))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/11 13:57